# Nano Level Associative Memories With Exploration Of Memristors

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**Abstract:** - Associative Memories (AMs) are crucial units for brain-like brilliant computing with applications in unreal goal, speech identification, artificial intelligence, and robotics. Computation with such applications generally trusts on spatial and temporal connections in the input signal and has to be robust against noise and incomplete practices. The schematic approach for applying AMs is through Artificial Neural Networks (ANNs). Raising the density of ANN grounded on traditional circuit components sets a challenge since devices achieve their physical scalability limits. Moreover, stored information in AMs is insecure to destructive input signals. New nano-scale elements, like memristors, comprise one solution to the density issue. Memristors are non-linear time-dependent circuit elements with an inherently small form element. Still, new neuromorphic circuits generally apply memristors to substitute synapses in schematic ANN circuits. This sub-optimal use is mainly as there's no proved design methodology to effort the memristor's non-linear attributes in a broader means. Index terms : associative memories (AMs), artificial neural networks (ANNs) , memristors, neuromorphic

## circuit .

#### INTRODUCTION

I.

The memristor was originally envisioned in 1971 as a missing non-linear passive two-terminal electrical component relating electric charge and magnetic flux linkage. According to the governing mathematical relations, the memristor's electrical resistance is not constant but depends on the history of current that had previously flowed through the device. The device remembers its history , that is, when the electric power is turned off, the memristor remembers its most recent resistance until it is turned on again. More recently, the definition has been generalized to cover all forms of two-terminal non-volatile memory devices based on resistance switching effect. The memristor is currently under development by various teams including Hewlett-Packard, SK Hynix and HRL Laboratories. These devices are intended for applications in nanoelectronic memories, computer logic and neuromorphic computer architecturtes.

#### II. RELATED WORKS

The real-world computational troubles now need to address with large quantities of less precision and uncertain data. An instance for such problems could be found in artificial intelligence which addresses with unifying computer vision, speech recognition, content and context recognition etc.(A.Engelbrecht et.al.,2002)[1]. Traditional computational patterns applied in numerical simulations, model fitting, data analysis etc. are inherently configured to figure out troubles that are precise and distinct. In addition, they lack the potential to find out from the complex relationships that exist in space and time. Therefore, conventional patterns are incompetent in resolving this category of problems. There's an progressive involvement in applying neuro-cortical models since aspiration for intelligent computing. Intelligent computing here relates to inference-based patterns which influence real world data and read/adapt while computation effects. The motive towards developing intelligent computing models is the human brain. In support, the BrainScaleS broadcast in Europe (M. Holler et.al., 1989)[15] and DARPA SyNAPSE program in the US (L. O. Chua et. al., 1976)[14] destine to gain new computing prototypes that exploit the reflections in biological nervous systems.

Associative Memories (AMs) are considered as crucial units for the human brain (Hodgkin and A. Huxley, 1990)[2]. Therefore, forcing from biological inspiration, AMs in intelligent computing are candidate units subject of memorization as well as seeing and adaptation. An AM block grounded on a tough circuit design might provide the realization of ranked models. We assumed memristor networks may be of value in robust nano-scale AM designs.

In this paper, we project a new methodology for applying AMs using memristors as circuit's elements The aim is to study the denser and more robust AM designs using memristor networks[17]. We assume that such network AMs might be more area-efficient than the conventional ANN designs if we may apply the memristor's nonlinear attribute for spatial and time-dependent temporary connection. An extensive simulation framework is built which applies Genetic Programming (GP) to develop AM circuits with memristor. The framework is grounded on the ParadisEO metaheuristics API and applies ngspice for the circuit rating. Our outcomes reveal that we may develop competent memristor-based networks that have the ability to put back customary ANNs used for AMs. We found AMs which a) may study spatial and temporal correlativity in the input signal b) optimize the trade-off between the size and the accuracy of the circuits; and c) are tough against destructive noise in the input signal. This robustness was attained at the expense of another factor in the network.

We have pointed that automatized circuit discovery is an anticipating tool for memristor based circuits. Later work will center on evolving circuits which may be applied as a unit for more complex sophisticated computing architectures.

## III. HIGH-LEVEL ASSOCIATIVE MEMORIES: BIOLOGICAL IMPLICATION

An Associative Memory (AM) has the ability to associate different memories to specific events. Such memories form an integral part of cognition in life forms, including humans. This ability allows the brain to react or adapt to external stimuli based on past experiences. The famous Pavlov experiments (W. Kantschik et. al., 2002) are a good example of associative memory: Pavlov observed that if a particular stimulus in the dog's surroundings was present when the dog was presented with meat powder, this stimulus would become associated with food and cause salivation on its own. The desired characteristics of associative memories have been summarized as follows:

- It should store many associated pattern pairs through a self-organizing process in a distributed manner.
- It should generate the appropriate response output response despite distorted or incompletely received inputs.
- It should dynamically append new associations to the existing stored memory.

Research in high-level AM models inherits these important properties along with biological plausibility and fast training times. Central to these ideas is the learning matrix , the Hopfield network , the bidirectional associative memory (BAM) , and the hierarchical temporal memory (HTM) . The learning matrix adapts the connection weights using a Hebbian learning rule[10]. In case of the Hopfield network[13], feedback creates a system which uses input and output patterns to represent its states. The BAM is similar to the Hopfield network, but has two layers of neurons, and additionally uses connection matrix to calculate both a) outputs given some inputs and b) inputs given a set of outputs. The HTM concept involves having a hierarchy of spatial and temporal operators with multiple nodes in each layer of the hierarchy. All nodes perform identical computations except for the top layer node, which has additional features for performing classification. The key aim of this paper is to develop a methodology to implement the functionality of AMs using memristor networks. AMs also form a specific area of research within self-organizing systems, commonly referred as Kohonen networks[16] or self-organized maps . Kohonen networks are rigorous mathematical models for two dimensional arrays of neurons, where the weight of each element corresponds to its coordinates in an ordered map. There are numerous application areas for high-level AMs within the intelligent computing paradigm, such as: pattern recognition, language learning, fact retrieval, inference and decision making, robotic controls etc.

## IV. CONCLUSION

- To sum up the core contribution of this paper:
- We would arise a general framework for projecting analog memristor-based circuits. GP approach normally has a tree kind data structure and therefore the mapping out is typically showed for one input and one output port circuits. This map would be widened in order to utilise GP for acquiring multiple input/output ports AM circuits.
- As our framework is in C++, the classes can well be extended or ported from one system to the other. The best node size is determined within the framework and has no hard bound limits.
- In the absence of a solid design technique, the basic criteria is to show that automatic circuit breakthrough is an anticipating instrument for memristor-based circuits. The results would indicate that one can efficiently apply composite facilitates with few elements.
- The primal result is that to develop effective memristor-based networks that possess the ability to put back the traditional artificial neural networks in use for associative memories.
- To develop associatory memories which may learn
- o spatial correlation between inputs and
- Temporal correlations inside the inputs stream.
- To explore the trade-off between the size and the accuracy of the circuits.
- To study the trade-off between the sizing and the accuracy of the circuits.
- To develop circuits which are strong against noise and variant on the input signal. This robustness might accomplish with some cost of extra nodes in the network.

### REFERENCES

- [1] A. Engelbrecht. Computational Intelligence, J. Wiley & Sons, New York, 2002
- [2] A. Hodgkin and A. Huxley, A quantitative description of membrane current and its application to conduction and excitation in nerve, Bulletin of Mathematical Biology, 52:25–71, 1990. 10.1007/BF02459568
- [3] A. Johannet, L. Personnaz, G. Dreyfus, J.-D. Gascuel, and M.Weinfeld. Specification and implementation of a digital Hopfield-type associative memory with on-chip training, Neural Networks, IEEE Transactions on, 3(4):529–539,1992
- [4] A. Liefooghe, L. Jourdan, and E. G. Talbi, A Unified Model for Evolutionary Multiobjective Optimization and its Implementation in a General Purpose Software Framework: ParadisEO-MOEO. url: http://paradiseo.gforge.inria.fr/. Rapport de recherche RR-6906, INRIA, 2009
- [5] B. Kosko. Bidirectional associative memories, Systems, Man and Cybernetics, IEEE Transactions on, 18(1):49–60, 1988.
- [6] CMOL/CMOS circuits: A design space exploration. In NORCHIP, pages 1–8, 2009.
- [7] D. George and J. Hawkins. A hierarchical bayesian model of invariant pattern recognition in the visual cortex, In Neural Networks, 2005, IJCNN '05, Proceedings, 2005 IEEE International Joint Conference on, volume 3, pages 1812–1817, 2005
- [8] D. Hammerstrom and M. S. Zaveri. Prospects for building cortex-scale
- [9] D. Hammerstrom, W. Henry, and M. Kuhn. The CNAPS architecture for neural network emulation, Parallel Digital Implementations of Neural Networks, pages 107–138, 1993.
- [10] D. O. Hebb. The organization of behavior, pages 43–54. MIT Press, Cambridge, MA, USA, 1988
- [11] E. Eiben. Introduction to Evolutionary Computing, Springer, Berlin, 2003
- [12] F. H. Bennett III, J. R. Koza, M. A. Keane, J. Yu, W. Mydlowec, and O. Stiffelman. Evolution by means of genetic programming of analog circuits that perform digital functions, In GECCO-99: Proceedings of the Genetic and Evolutionary Computation Conference, July, volume 1317, pages 1477–1483, 1999.
- [13] J. J. Hopfield. Neural networks and physical systems with emergent collective computational abilities, Proceedings of the National Academy of Sciences, 79(8):2554–2558, 1982.
- [14] L. O. Chua and Sung. M. K. Memristive devices and systems. Proceedings of the IEEE, 64(2); 209-223, 1976.
- [15] M. Holler, S.Tam, H. Castro and R.Benson, An electrically trainable artificial neural network (etnn) with 10240 'floating gate' synapses, In neural networks, 1989. IJCNN., International Joint Conference on , pages 191-196, vol.2, 1989.
- [16] T. Kohonen. Self-Organization and Associative Memory, volu me 8, Springer Verlag, 1989.
- [17] J.Haugeland. Artificial Intelligence, MIT Press, Cambridge, 1985.